

What is claimed is:

- 1 1. A digital bus comprising:
2 a transmitter unit capable of generating a plurality of clock signals;
3 a receiver unit comprising:
4 one or more first-in-first-out (FIFO) units; and
5 a synchronizer unit coupled to the one or more FIFO units, the
6 synchronizer unit adapted to receive the plurality of clock signals, a sample clock
7 signal, and a reset signal and to generate a plurality of write reset signals and a
8 read reset signal, wherein each of the plurality of write reset signals has a latency
9 with respect to the read reset signal of less than or equal to one clock cycle; and
10 a transmission medium to couple the plurality of clock signals from the
11 transmitter unit to the receiver unit.
- 1 2. The digital bus of claim 1, wherein the transmitter unit comprises a transceiver.
- 1 3. The digital bus of claim 2, wherein the transceiver comprises a processor.
- 1 4. The digital bus of claim 1, wherein each of the plurality of clock signals
2 comprises a pair of complementary clock signals.
- 1 5. The digital bus of claim 4, wherein the pair of complementary clock signals have
2 a skew of less than 90 degrees.
- 1 6. The digital bus of claim 4, wherein each of the plurality of clock signals has a
2 frequency of between about 500 megahertz and about five gigahertz.
- 1 7. The digital bus of claim 1, wherein the transmission medium comprises a cable.

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1 8. The digital bus of claim 1, wherein each of the plurality of clock signals has a
2 clock frequency and the sample clock has a sample clock frequency that is about twice
3 the clock frequency.

1 9. The digital bus of claim 1, wherein the transmission medium comprises a plurality
2 of metal interconnects formed on a substrate.

1 10. The digital bus of claim 1, wherein the transmission medium comprises free
2 space.

1 11. The digital bus of claim 1, wherein the receiver unit comprises a memory unit.

1 12. The digital bus of claim 11, wherein the memory unit comprises a dynamic
2 random access memory.

1 13. An integrated circuit comprising:
2 a transmitter unit capable of generating a plurality of clock signals;
3 a receiver unit comprising:
4 one or more first-in-first-out (FIFO) units; and
5 a synchronizer unit coupled to the one or more FIFO units, the
6 synchronizer unit adapted to receive the plurality of clock signals and a sample
7 clock signal and to generate a plurality of write reset signals and a read reset
8 signal, wherein each of the plurality of write reset signals has a latency with
9 respect to the read reset signal of less than or equal to one clock cycle; and
10 a transmission medium to couple the plurality of clock signals from the
11 transmitter unit to the receiver unit.

1 14. The integrated circuit of claim 13, wherein the transmitter unit, the receiver unit,
2 and the transmission medium are fabricated on a single substrate.

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1 15. The integrated circuit of claim 14, wherein the single substrate is silicon.

1 16. The integrated circuit of claim 13, wherein the transmission medium comprises a
2 plurality of copper interconnects.

1 17. The integrated circuit of claim 13, wherein the transmitter unit comprises a
2 memory unit.

1 18. The integrated circuit of claim 17, wherein the memory unit comprises a dynamic
2 random access memory.

1 19. The integrated circuit of claim 17, wherein the memory unit comprises a static
2 random access memory.

1 20. A synchronizer unit comprising:
2 a logic circuit adapted to receive a plurality of clock signals, a reset signal, and a
3 sample clock signal and to generate a synchronized reset signal synchronized to the reset
4 signal, a plurality of write reset signals, and a read reset signal synchronized to the
5 plurality of write reset signals, the read reset signal having a latency with respect to each
6 of the plurality of write reset signals of less than or equal to one clock cycle.

1 21. The synchronizer unit of claim 20, wherein the logic circuit comprises
2 complementary metal-oxide semiconductor logic circuits.

1 22. The synchronizer unit of claim 21, wherein the logic circuit comprises a plurality
2 logic gates having a delay of less than about two nanoseconds.

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- 1 23. A synchronizer unit comprising:
2 a first synchronizer unit to receive a plurality of clock signals and a reset signal
3 and to generate a synchronized reset signal;
4 a second synchronizer unit to receive the plurality of clock signals and the
5 synchronized reset signal and to generate a plurality of write reset signals; and
6 a third synchronizer unit to receive a sample clock signal, the synchronized reset
7 signal, and the plurality of write reset signals and to generate a read reset signal having a
8 latency with respect to each of the write reset signals of less than or equal to one clock
9 cycle.
- 1 24. The synchronizer unit of claim 23, wherein the first synchronizer unit comprises a
2 plurality of clock signal paths, wherein each of the plurality of clock signal paths
3 comprises a plurality of serially connected flip-flops.
- 1 25. The synchronizer unit of claim 24, further comprising an OR gate coupled to each
2 of the plurality of clock signal paths, the OR gate having an output node providing the
3 synchronized reset signal.
- 1 26. The synchronizer unit of claim 24, wherein the second synchronizer unit
2 comprises a plurality of clock signal paths, wherein each of the plurality of clock signal
3 paths comprises a plurality of serially connected flip-flops.
- 1 27. A method of forming a read reset signal, the method comprising:
2 synchronizing a first reset signal to a plurality of clock signals to form a
3 synchronized reset signal;
4 synchronizing the synchronized reset signal to the plurality of clock signals to
5 form a plurality of write reset signals; and

6 synchronizing the synchronized reset signal to a sample clock signal to form a
7 read reset signal having a latency with respect to each of the plurality of write reset
8 signals of less than or equal to one clock cycle.

1 28. The method of claim 27, wherein synchronizing a first reset signal to a plurality of
2 clock signals to form a synchronized reset signal comprises:

3 clocking the first reset signal into a plurality of parallel flip-flops using the
4 plurality of clock signals to clock each of the plurality of parallel flip-flops to form a
5 plurality of clocked reset signals; and

6 ORing the plurality of clocked reset signals to form the synchronized reset signal.

1 29. The method of claim 27, wherein synchronizing the synchronized reset signal to
2 the plurality of clock signals to form a plurality of write reset signals comprises:

3 clocking the synchronized reset signal into a plurality of parallel flip-flops using
4 the plurality of clock signals to clock each of the plurality of parallel flip-flops to form
5 the plurality of write reset signals.

1 30. The method of claim 27, wherein synchronizing the synchronized reset signal to a
2 sample clock signal to form a read reset signal having a latency with respect to each of
3 the plurality of write reset signals of less than or equal to one clock cycle comprises:

4 adjusting a number of flip-flops in a signal path such that the read reset signal
5 with respect to each of the plurality of write signals has a latency of less than or equal to
6 one clock cycle.

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